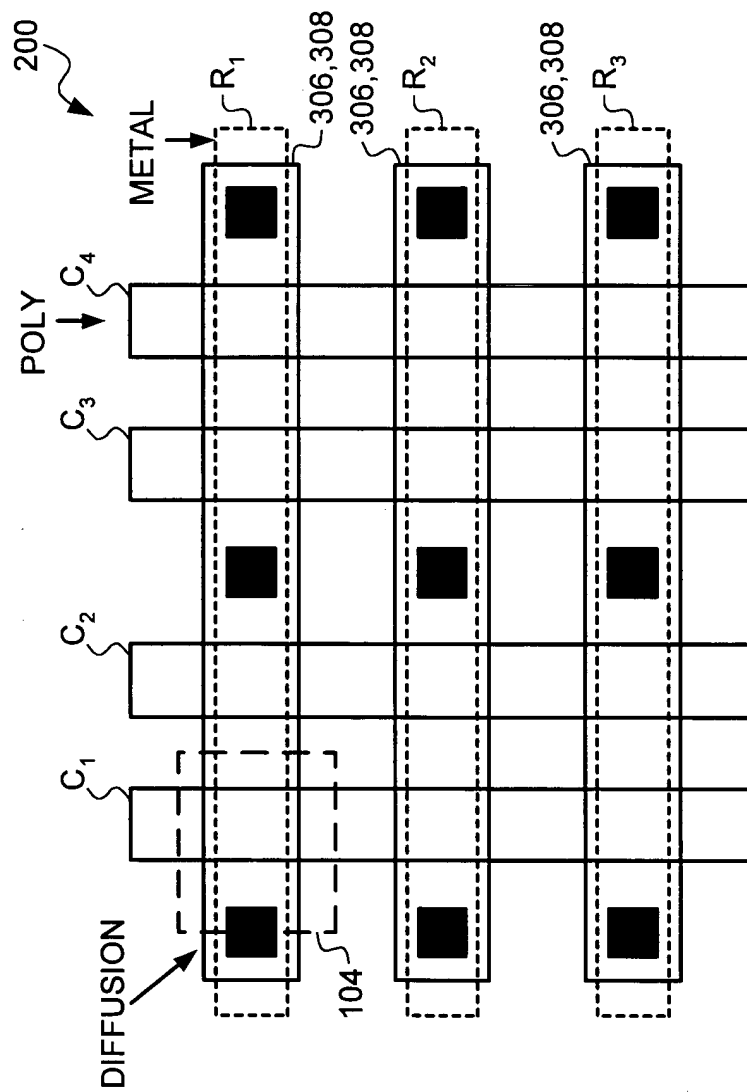


FIGURE 1



## FIGURE 2

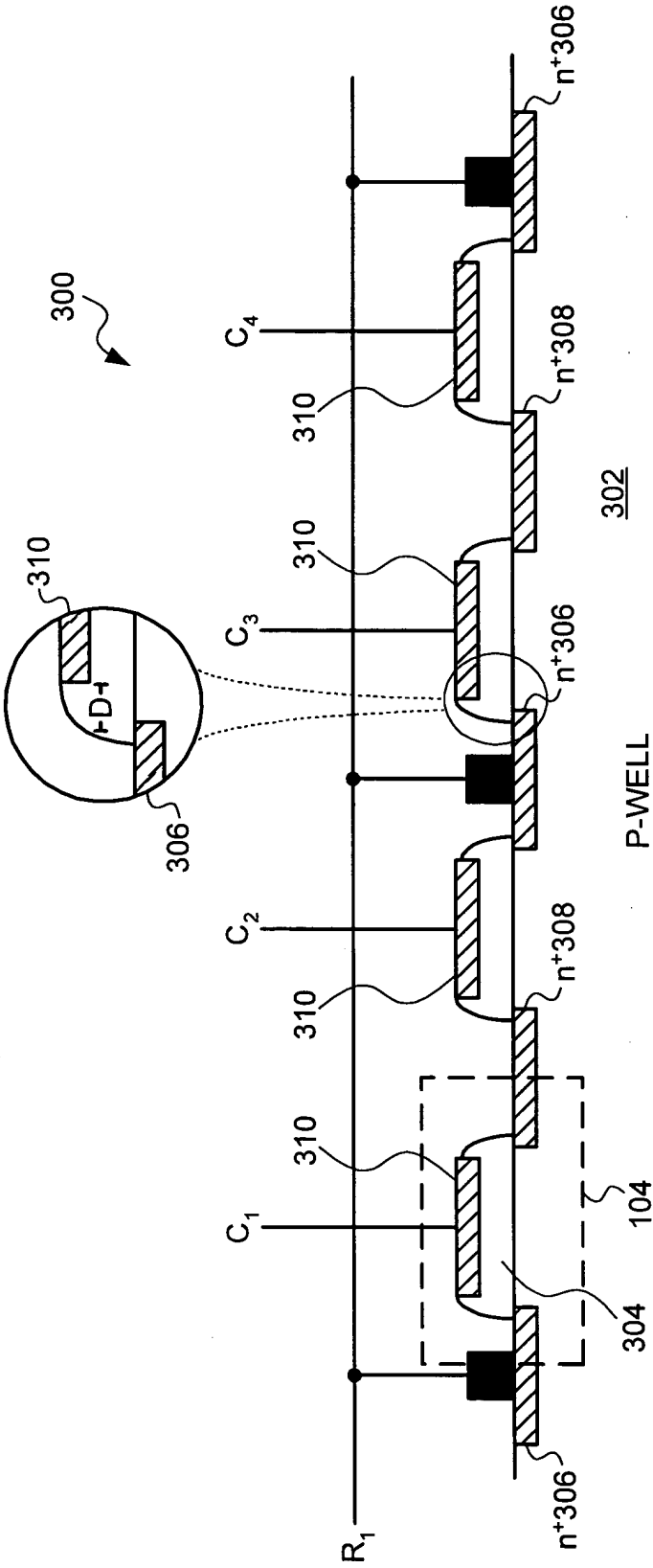


FIGURE 3

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	8	0	YES	401
	SC/UR	8	8	NO	403
	UC/SR	3.3	0	NO	405
	UC/UR	3.3	8	NO	407
				ISENSE	
READ	SC/SR	1.8	0	YES	409
	SC/UR	1.8	1.8	NO	411
	UC/SR	0	0	NO	413
	UC/UR	0	1.8	NO	415

FIGURE 4

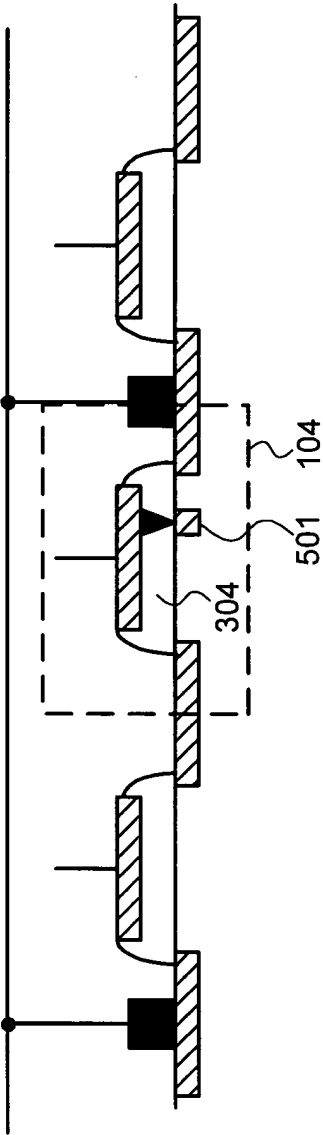


FIGURE 5

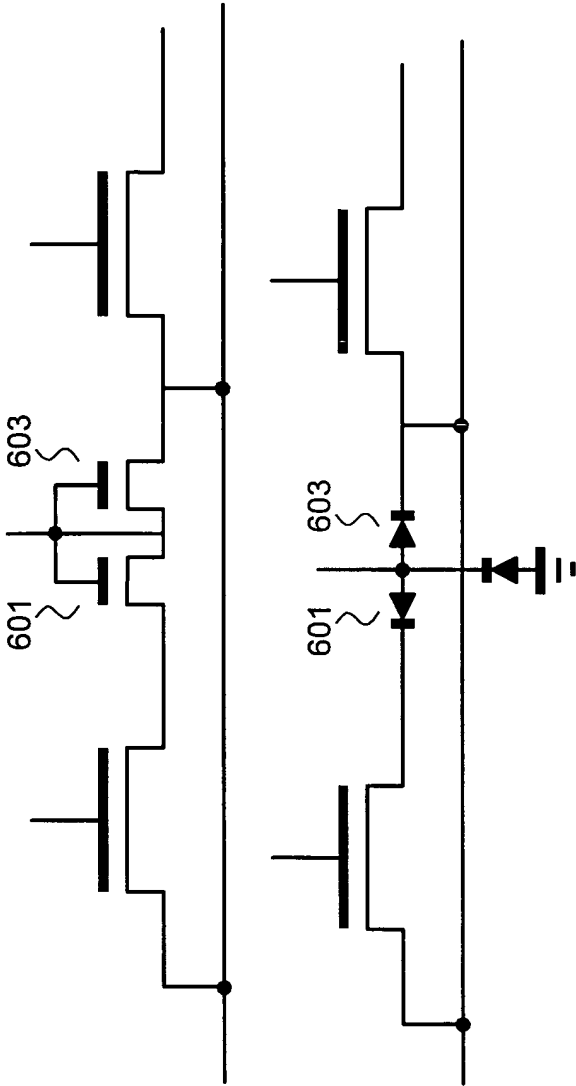
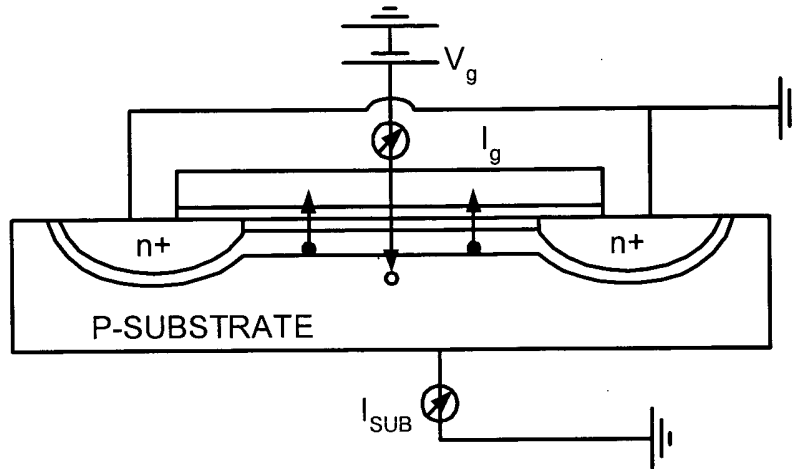
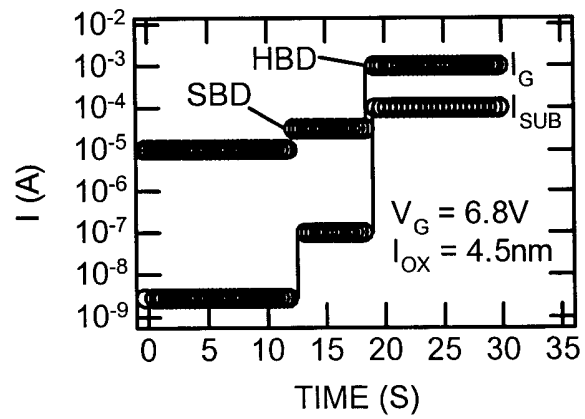
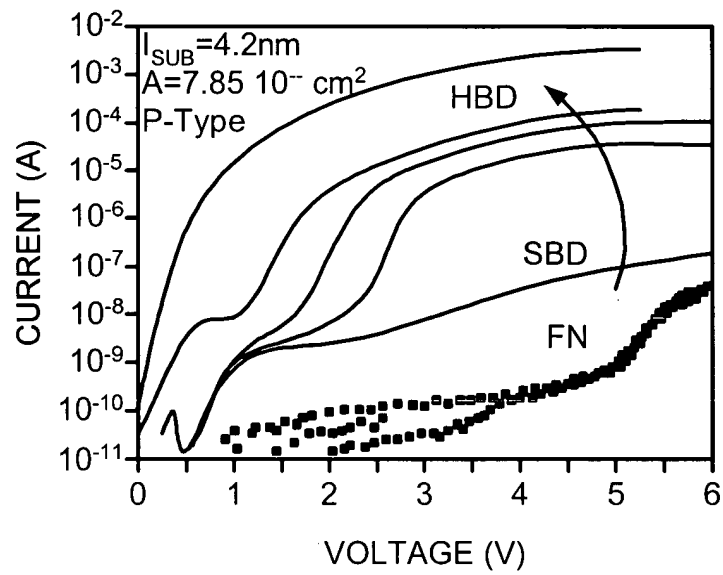


FIGURE 6

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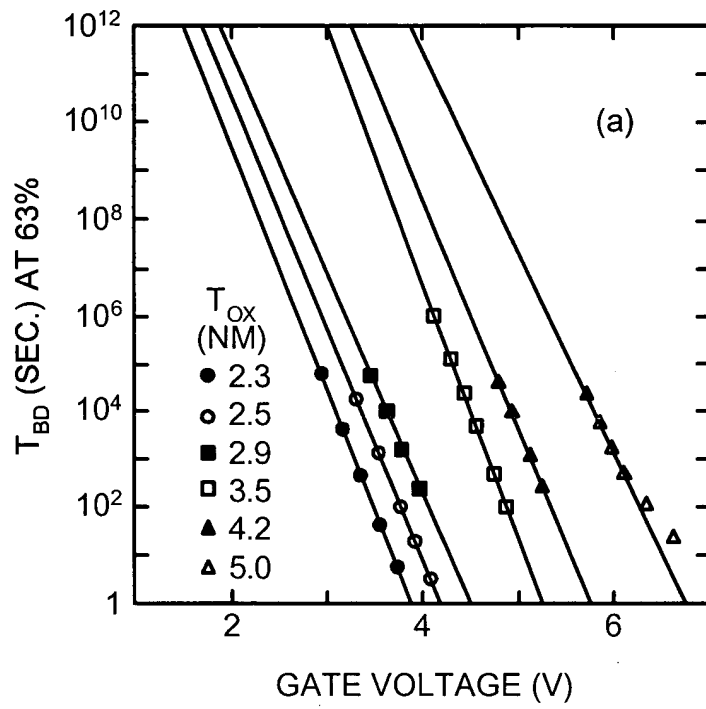
**FIGURE 7****FIGURE 8**

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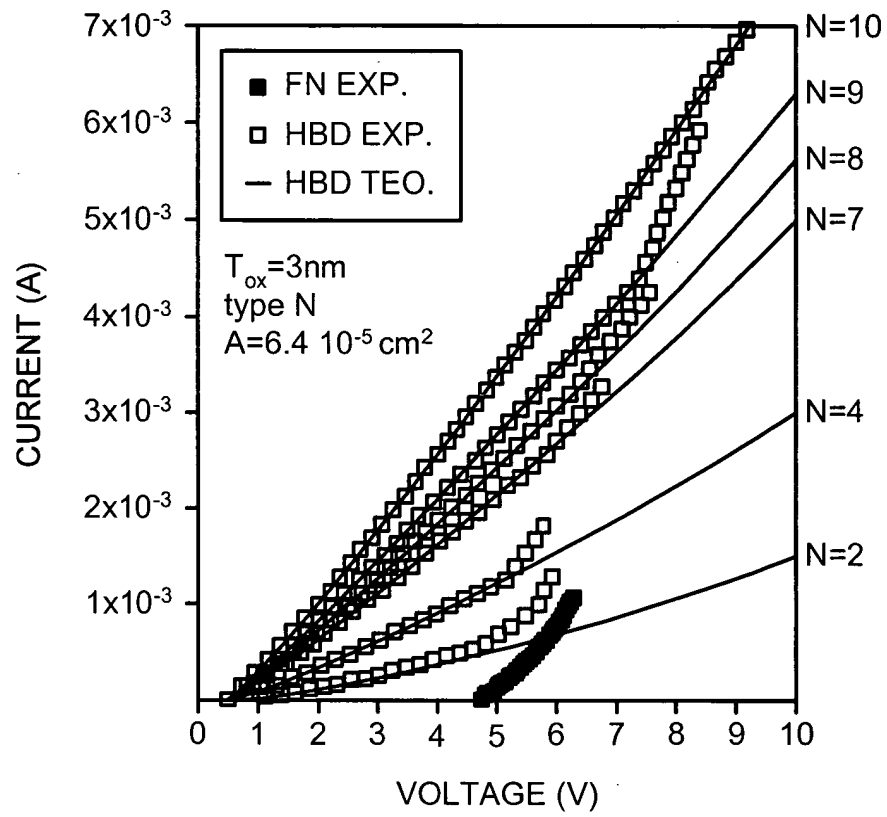
**FIGURE 9**



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**FIGURE 10**

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**FIGURE 11**

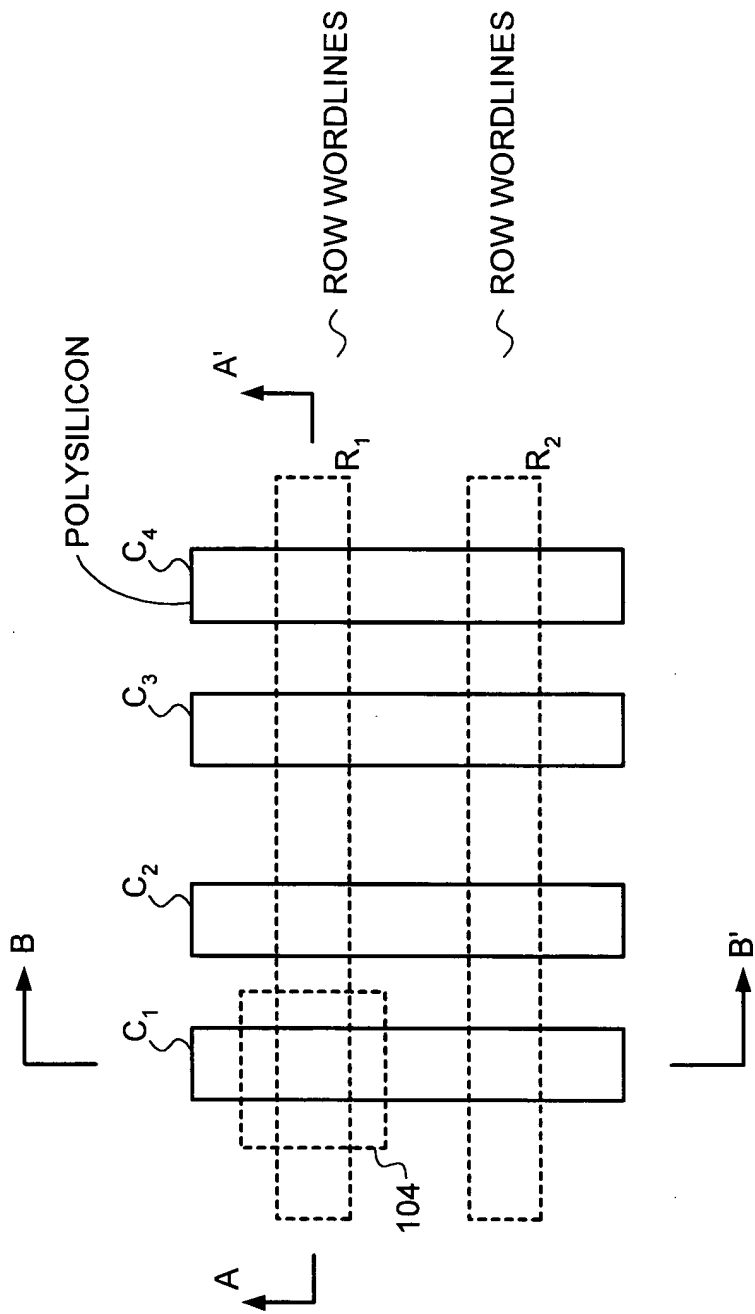
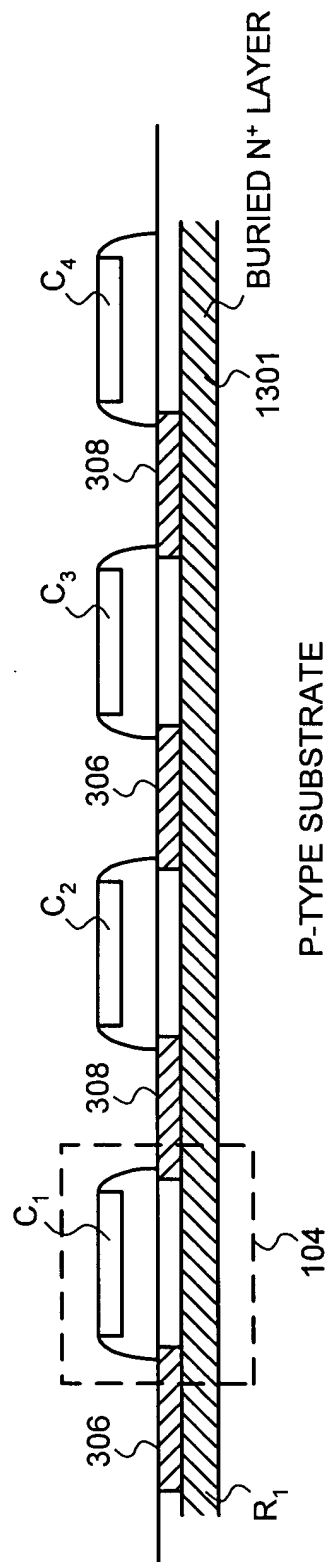
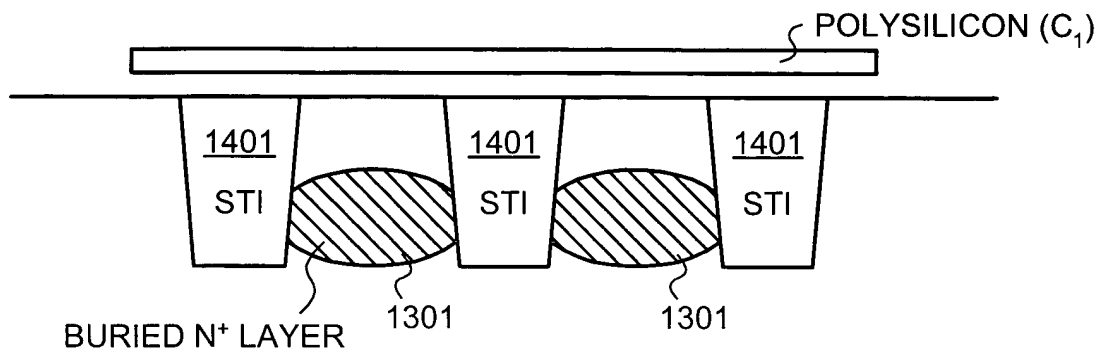


FIGURE 12

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**FIGURE 13**

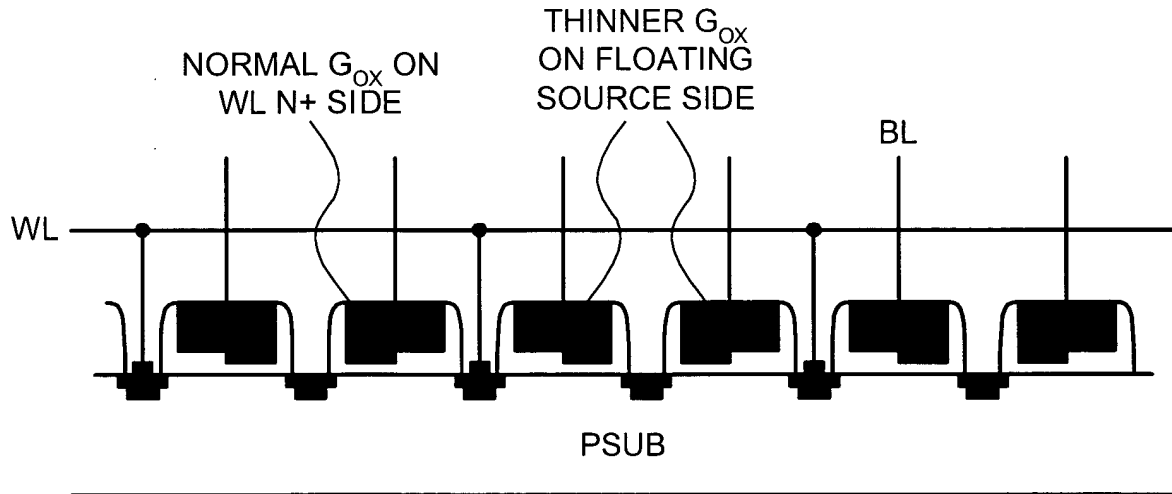
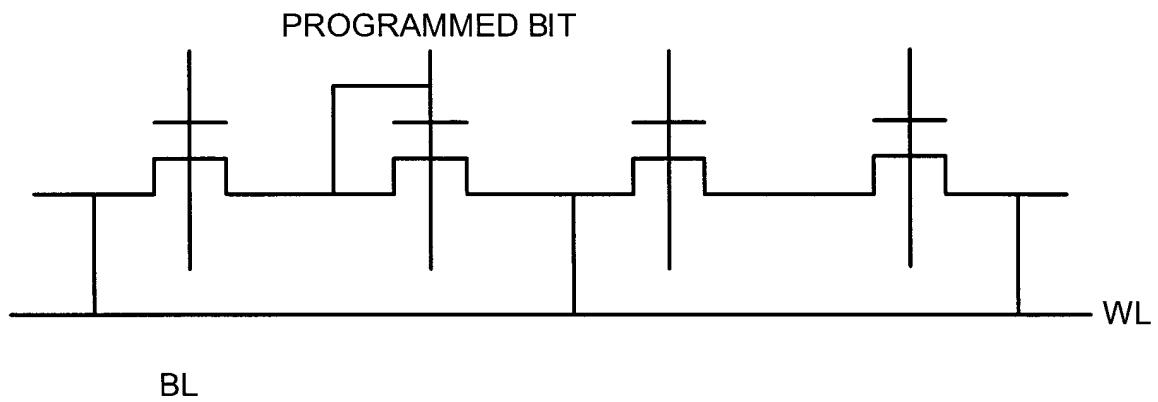


**FIGURE 14**

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	V <sub>PP</sub>	0	YES	401
	SC/UR	V <sub>PP</sub>	FLOATING	NO	403
	UC/SR	< 0.5 V	0	NO	405
	UC/UR	< 0.5 V	FLOATING	NO	407
				I <sub>SENSE</sub>	
READ	SC/SR	V <sub>DD</sub> OR V <sub>CC</sub>	0	YES	409
	SC/UR	V <sub>DD</sub> OR V <sub>CC</sub>	V <sub>DD</sub> OR V <sub>CC</sub>	NO	411
	UC/SR	0 OR FLOAT	0	NO	413
	UC/UR	0 OR FLOAT	V <sub>DD</sub> OR V <sub>CC</sub>	NO	415

FIGURE 15

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**FIGURE 16****FIGURE 17**

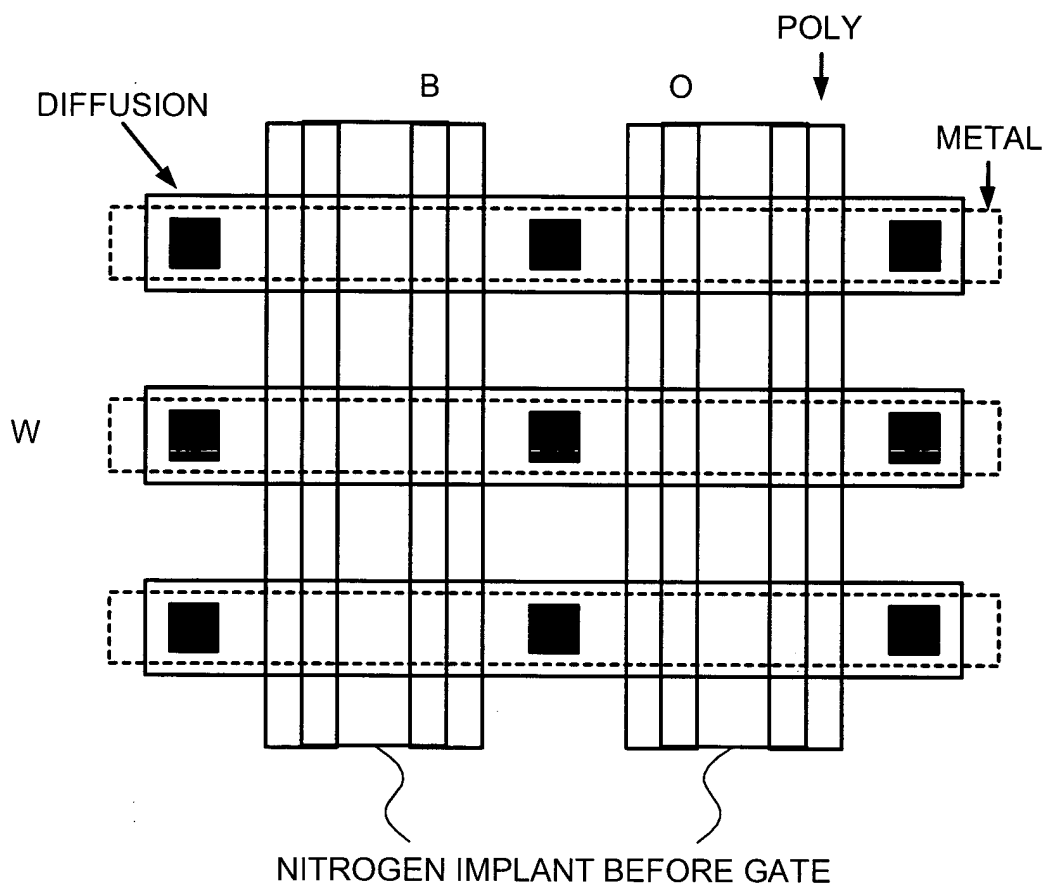
0.18um/0.13um XPM CX CELL OPERATION

		VBL (V)	VWL (V)	PROGRAM
PROGRAM	SB/SW	$V_{PP}$	0	YES
	SB/UW	$V_{PP}$	PC TO $V_{PP}/2$ AND FL	NO
	UB/SW	$< 0.5\text{ V}$	0	NO
	UB/UW	$< 0.5\text{ V}$	PC TO $V_{PP}/2$ AND FL	NO
				$I_{SENSE}$
READ	SB/SW	$V_{DD}$ OR $V_{CC}$	0	YES
	SB/UW	$V_{DD}$ OR $V_{CC}$	$V_{DD}$ OR $V_{CC}$	NO
	UB/SW	0	0	NO
	UB/UW	0	$V_{DD}$ OR $V_{CC}$	NO

$V_{PP}$  = 8~9V FOR  $G_{OX}=32A$  (0.18um) OR 5-7 FOR  $G_{OX}=20A$ , OR 3~4.5 V  
FOR 10-15A (5 TO 10A THINNER THAN NORMAL STANDARD GATE OXIDE).  
 $V_{DD}$  = I/O VOLTAGE 3.3V OR 2.5V  
 $V_{CC}$  = 1.8V FOR 0.18um AND 1.2V FOR 0.13um

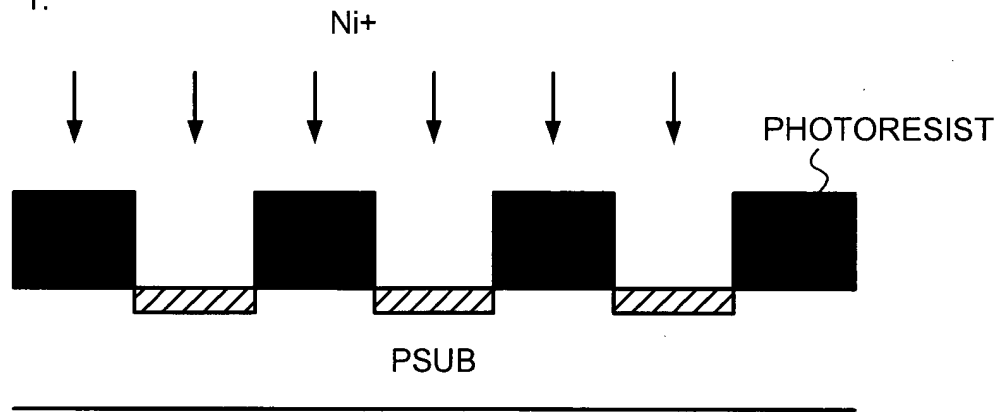
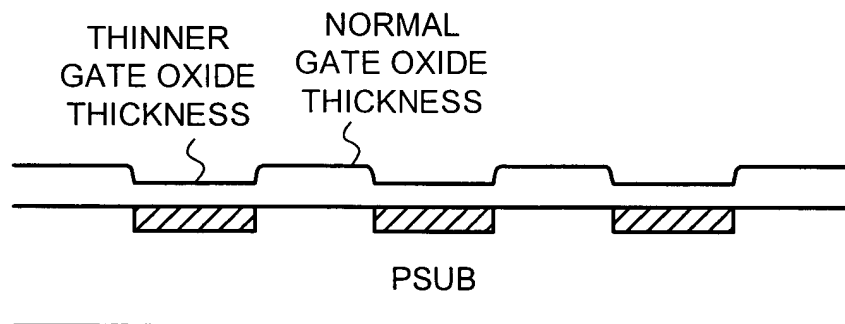
FIGURE 18



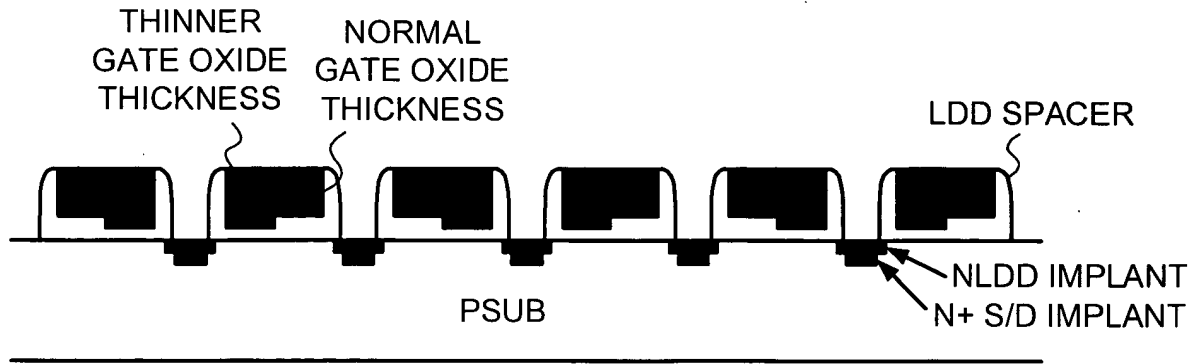
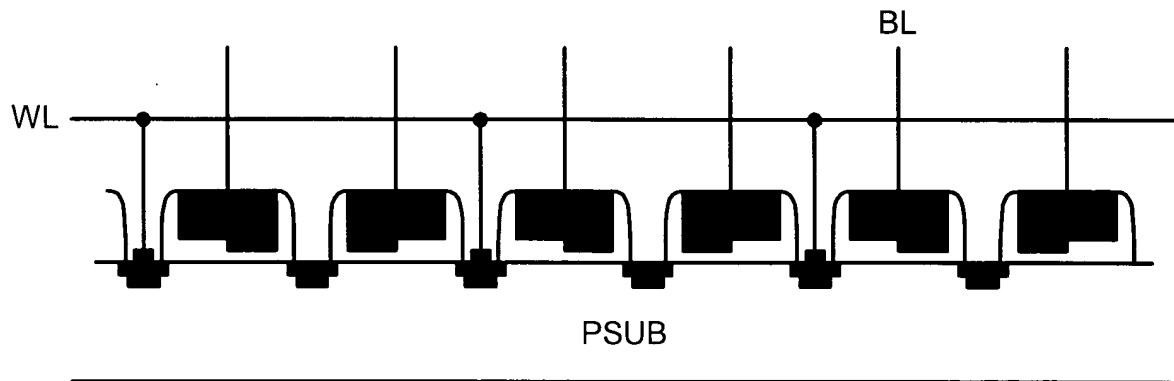


**FIGURE 19**

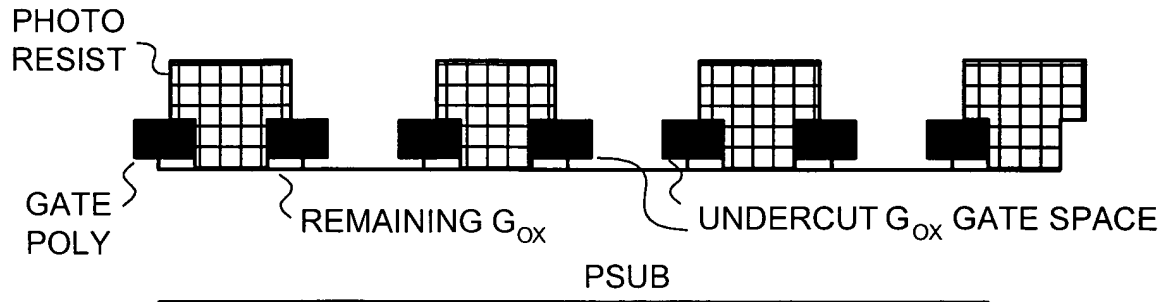
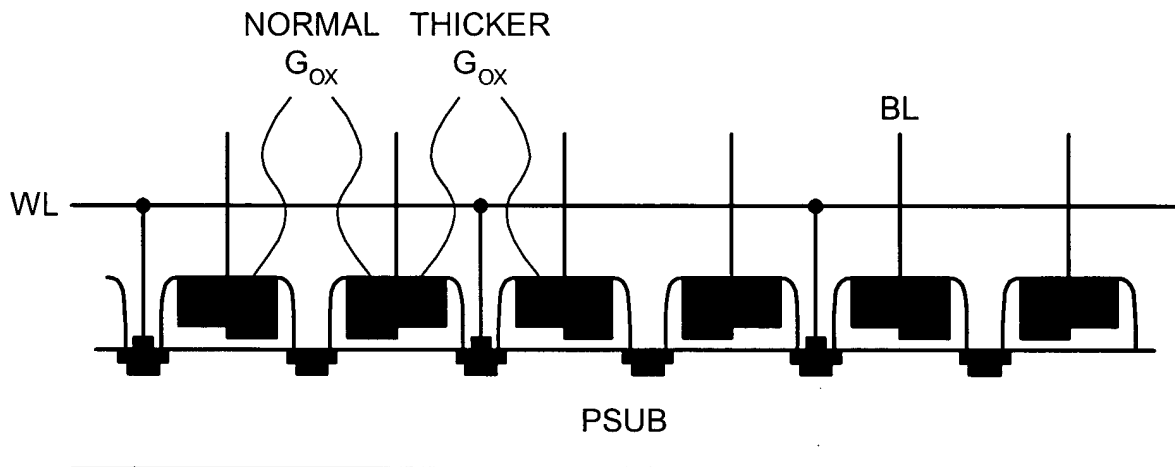
STEP 1:

**FIGURE 20****FIGURE 21**

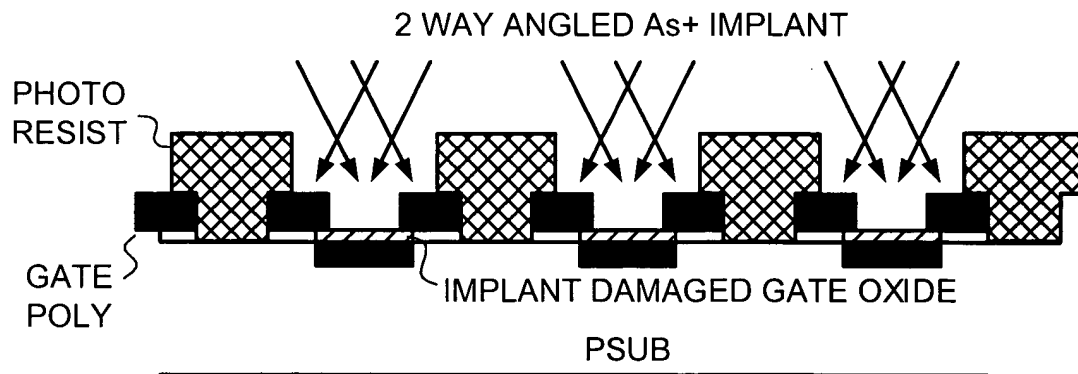
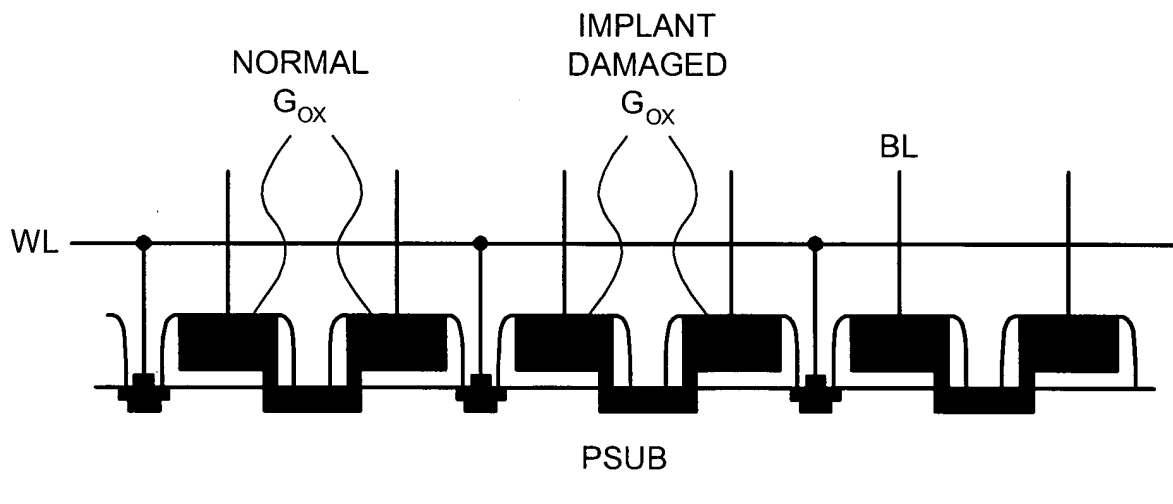
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**FIGURE 22****FIGURE 23**

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**FIGURE 24****FIGURE 25**

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**FIGURE 26****FIGURE 27**